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Product :	ETKS-3.0, ETK-S3.0_SET			
Title :	Change Information			
File :	ETKS3.0_Change_Information_V04.doc			
TTN :	F-00K-104-060, F-00K-104-304			
Comments :	Currently shipped: 25C010 FPGA version: V25 Hardware-state: C010			
Created:	Name Higgins	Department ETAS-PHW/EES1	Signature Higgins	Date 04.12.2009
Released:	Name Collins	Department ETAS-PHW/EES22	Signature Collins	Date 04.12.2009
C h a n g e s				
Revision	Description	Date	Name	Signature
01	21B010- Initial version	18.08.2005	Higgins	Higgins
02	23C010- FPGA update: Brain Dead Flashing Hardware update: Removed PCB trace on Reset signal	12.01.2006	Higgins	Higgins
03	24C010- FPGA update: Added Trigger Direct Measurement, updated ECU reset monitoring behavior, reduced current feedback on JTAG signals	04.12.2007	Higgins	Higgins
04	25C010- FPGA update: Removed initialization of Nexus Port Configuration Register (PCR).	04.12.2009	Higgins	Higgins

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1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.

Two different items are described.

- Explanation of the version-system of the ETK-S3.0
- The required versions of software (INCA / ASCET / INTECRIO), HSP (calibration hardware firmware of e.g. ES59x, ES690, ES1232, ...) and ETK - hardware. Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

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2 Tool-Chain Information

2.1 Version-Syntax of the ETK-S3.0

The ETK-S3.0 version information is located on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax: **aacddd/ee**

PLD-Code Information:

aa: FPGA-Code version (10, 11, 12...) see chapter 3

Hardware-Information:

d: PCB version (A, B, C, ...)

ddd: Hardware state of the PCB (010, 011, 012, ...) see chapter 4

ee: Assembly variant of the PCB (00, 01, 02, ...)

The first delivered hardware state of the ETK-S3.0 was **21B010/00**.

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2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.

If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	Needed version	Remarks
HSP	V5.0	Note: HSP V6.1 required to configure new Reset monitoring mechanism or used trigger direct measurement introduced with HDC v2.4
ES690	V10.0.2	Supported
ES59x	V10.0.2	Supported
ES910.2	HSP V5.1.1	Supported
ES1000.2/3 – system	V10.0.2	Supported with ES1232
MAC2, ES1000.1, ES1200/01, and ES1231		Not supported
Software		
INCA	V5.4	Note: INCA V6.1 required to configure new Reset monitoring mechanism or used trigger direct measurement introduced with HDC v2.4
ASCET-RP	V5.4.1	
INTECRIO	V2.0	

List of officially supported Freescale microcontrollers:

- MPC5534
- MPC5554
- MPC5553
- MPC5565
- MPC5566
- MPC5567
- MPC5674F (FPGA v2.5 required)

The registered user will automatically receive the newest INCA-version (CD-ROM)
Updates or refreshes can be downloaded from the ETAS homepage:

<http://de.etasgroup.com>

<http://en.etasgroup.com>

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3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code within the ETK-S3.0 is stored onto programmable logic devices (FPGA). The FPGA-code starts with version 2.1. For the version syntax please refer to chapter 2.1.

3.2 FPGA-Code version 2.1 was the first delivered version

3.2.1 Details of change

Version 2.1: Initial version, dated August 18, 2005

Version 2.3: Update file dated January 12, 2006
Issue: Request for Brain Dead Flashing Support
Remedy: New FPGA file

Version 2.4: Update file dated December 4, 2007
Issue: Request for new reset monitoring mechanism and Triggered Direct Measurement support. Report of current back feeding on JTAG pins under special conditions while the ECU is powering down.
Remedy: New FPGA file

Version 2.5: Update file dated October 1, 2009
Issue: Remove setup of the Nexus PCR register to avoid setting invalid values on future microcontroller versions.
Remedy: New FPGA file

Attention: For updating the ETK - HDC with a later version by using the ETK - configuration tool, all ETK - FPGA - packages will be updated one after another and will last a few minutes.

3.2.2 Delivery condition

The FPGA version **2.5** will be programmed into all new shipments.

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4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the manufacturing of this ETK. Information about the changes is listed underneath. The hardware-state starts with version B010. For the version syntax please refer to chapter 2.1.

4.2 Hardware version B010 was the first delivered version

4.2.1 Details of change

Version B010: Initial version

Version C010:

Issue: Debugger Reset pin connected to FPGA without 5V protection.

Remedy: Remove trace to FPGA, leave trace to ECU connector.

4.2.2 Delivery condition

The hardware-state **C010** will be delivered with all new shipments.
ETKs with 'older' hardware-states can not be modified to the current valid state.

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5 Abbreviations

ETK	Emulator test probe
ES1000	VME - system, successor of INCA-VME
INCA-VME	Old VME - system for MC and RP
ES690	MC hardware, successor of MAC2
MAC2	Old MC hardware
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	H ardware S ervice P ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	M easurement & C alibration
RP	R apid P rototyping
PLD	P rogrammable L ogic D evice
FPGA	F ree P rogrammable G ate A rray; interface component to the application hardware
PCB	P rinted C ircuit B oard